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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/664,094	09/19/2000	Masayuki Mizuno	Q60884	5281

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/664,094	MIZUNO, MASAYUKI	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE on 5.3.04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5 and 9-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5 and 9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/03/2004 has been entered.

Response to Amendment

After-Final Amendment filed 03/05/2004 has been entered following aforementioned Request for Continued Examination. In said Amendment Applicant substantially amended claims 1, 2, 5, 9, 10 and 11. Applicant canceled claims 3-4, 6-8 and 12. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Drawings

The examiner has approved the Amendment to the Drawings filed 3/5/04.

Response to Arguments

2. Applicant's arguments filed 03/05/2004 have been fully considered but they are not persuasive. In particular, in view of the substantially amended claim language of claims 1, 2 and 9-11 new rejections are provided for these claims. Applicant traverses the rejection under 102(b) over Phelan on the grounds that neither "the upper nor lower

strip conductors 15 are disclosed as containing a respective through hole" (page 11-12 of Remarks). However, strip conductor 15 is taught as a single entity and moreover, "through hole" in common language means hole throughout ("from one side to the other", cf. Merriam-Webster's Collegiate Dictionary, tenth Edition, page 1230 (1999) (ISBN: 0-87779-708-0)), which is met by the hole shown in 15 in Figure 4 by Phelan. A further limitation is needed should Applicant wish to distinguish his hole from Phelan's. In view of the above, the rejection of claim 5 over Phelan under 102(b) is made to stand. Finally, while Figures 2 and 3 disclose the further limitation "wherein an aperture size of said through hole is smaller than a width of said signal line", Applicant should provide the verbal disclosure for it by amendment of the Specification.

Specification

3. The disclosure is objected to because of the following informalities: the further limitation newly introduced by aforementioned Amendment, i.e., "wherein an aperture size of said through hole is smaller than a width of said signal line", although evident from Figures 1 and 2, should be included also in the actual text of the Specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. ***Claim 5*** is rejected under 35 U.S.C. 102(b) as being anticipated by Phelan (3,771,075). Phelan teaches (cf. Figure 2):

a signal line 10 (cf. column 2, lines 37-49);

a ground plate 13 (cf. column 2, lines 37-49); and

another signal line 11 (cf. column 2, lines 37-49) close to said signal line and on an opposite side of said ground plate;

wherein at least one through hole is formed in said signal line, i.e., conductive strip 15 constituting the signal lines 10 and 11 (cf. column 2, line 52) showing a through hole, i.e., a hole through a layer, i.e., through conductive strip 15 taught as a single entity; and an inner wall of said through hole formed in said signal line is only directly electrically connected to said signal line by virtue of being an interruption of conductive matter; and

wherein at least one through hole 14 (cf. column 2, line 49) is formed in said ground plate; and an inner wall is only directly electrically connected to said signal line by virtue of being a slot, i.e., open space (cf. column 3, lines 15-20).

Finally, a characteristic impedance of said transmission line is increased by any hole, because the result of any hole in a transmission line is a reduction of capacitance (because less main surface area available) and an increase in inductance (because charge carriers are further hampered in their ability to quickly respond to any imposed electric field, said charge carriers having to circumnavigate the hole area), and hence the characteristic impedance defined by $\sqrt{}$ (L/C) is necessarily increased as a result said any hole.

6. ***Claims 9-11*** are rejected under 35 U.S.C. 102(b) as being anticipated by Fuchida et al (5,723,908). Fuchida et al teach (cf. title, abstract, Figures 8A, 8B, 12B) a signal line 10 (cf. 6, l. 62 – col. 7, l. 13; see also signal line 1 as described in col. 4, l. 66 – col. 5, l. 10); a ground plate 20 (cf. col. 62 – col. 7, l. 13; see also ground plate 2 as described in col. 4, l. 66 – col. 5, l. 10), and another signal line 30 (cf. col. 6, l. 62 – col. 7, l. 13) disposed on an opposite side of said ground plate as said signal line (see col. 6, l. 64-67); wherein a plurality of slit holes are formed (cf. Figure 12B) by forming said signal line or said ground plate (cf. ground plate 2 of Fig. 12B) of a plurality of thin strips and by connecting the thin strips at respective terminal ends of the thin strips (cf. Fig. 12B: the thin strips are connected at respective terminal ends to the left and right of said slits), and an inner wall of said plurality of slit holes is directly electrically connected to said signal line (because said inner wall is completely coated with the filling of the slits, which is interlayer insulating film 15 (cf. col. 5, l. 33)). In conclusion, Fuchida et al anticipate claim 9.

On claim 10: Fuchida et al teach (cf. title, abstract, Figures 8A, 8B, 12B) a signal line 10 (cf. 6, l. 62 – col. 7, l. 13; see also signal line 1 as described in col. 4, l. 66 – col. 5, l. 10); a ground plate 20 (cf. col. 62 – col. 7, l. 13; see also ground plate 2 as described in col. 4, l. 66 – col. 5, l. 10), another signal line 30 (cf. col. 6, l. 62 – col. 7, l. 13) disposed on an opposite side of said ground plate as said signal line (see col. 6, l. 64-67); wherein a plurality of through holes are formed in said signal line (cf. Figures 4B and 12B: the wiring pattern 11 of which the ground plate and signal line consist (cf. col. 5, l. 5-33) has through holes because interlayer insulation layer 15 constitutes a through

hole in said wiring pattern 11 (cf. Figure 4B)), and an inner wall of said plurality of through holes is directly electrically connected to said signal line (because said inner wall is completely coated with the filling of the slits, which is interlayer insulating film 15 (cf. col. 5, l. 33)). In conclusion, Fuchida et al anticipate claim 10.

On claim 11: Fuchida et al teach (cf. title, abstract, Figures 8A, 8B, 12B) a signal line 10 (cf. 6, l. 62 – col. 7, l. 13; see also signal line 1 as described in col. 4, l. 66 – col. 5, l. 10); a ground plate 20 (cf. col. 62 – col. 7, l. 13; see also ground plate 2 as described in col. 4, l. 66 – col. 5, l. 10), another signal line 30 (cf. col. 6, l. 62 – col. 7, l. 13) disposed on an opposite side of said ground plate as said signal line (see col. 6, l. 64-67); wherein a plurality of through holes are formed in said ground plate (cf. Figures 4B and 12B: the wiring pattern 11 of which the ground plate and signal line consist (cf. col. 5, l. 5-33) has through holes because interlayer insulation layer 15 constitutes a through hole in said wiring pattern 11 (cf. Figure 4B)), and an inner wall of said plurality of through holes is directly electrically connected to said ground plate (because said inner wall is completely coated with the filling of the slits, which is interlayer insulating film 15 (cf. col. 5, l. 33)). In conclusion, Fuchida et al anticipate claim 11.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. ***Claim 1*** rejected under 35 U.S.C. 103(a) as being unpatentable over Steensma (3,925,740) (previously made of record) in view of MacDonald (5,633,613) (previously made of record), Kuroda et al (5,479,138) and Buuck et al (5,568,107).

Steensma teaches a semiconductor integrated circuit comprising a microstrip structure (cf. title and abstract), comprising: a signal line 3/8 (cf. column 1, line 67 and column 2, line 9), and a ground plate 2 (cf. column 1, line 66), wherein at least one through hole 7 (cf. column 2, line 6) is formed in said signal line, and an inner wall of said through hole is only directly electrically connected to said signal line by virtue of the non-conductive nature of a hole (otherwise there would not be a hole but merely a change in the electrical conductivity).

Steensma does not teach the further limitation of "another signal line disposed close to the signal line and on an opposite side of said ground plate" (henceforth called further limitation (a)), nor does Steensma teach the further limitation "wherein an aperture size of said through hole is smaller than a width of said signal line" (henceforth called further limitation (b)).

However, it would have been obvious to include said further limitation (a), because in the art of impedance tuning, i.,e., the art of Steensma (cf. col. 1, lines 5-15), the application of two transmission lines on opposite sides of a ground plane has long been recognized as a means to utilize the ground plane as an electrostatic shielding means, *as witnessed for instance by MacDonald*, who teaches signal lines 30 and 32 on opposite sides of ground plate 34 (cf. column 3, line 11 –column 4, line 30).

Motivation, for inclusion of the teaching by MacDonald in the invention by Steensma, stems from the added control on impedance of the transmission line (cf. abstract in MacDonald), which would have been an obvious improvement over the method by Steensma to tune the impedance of the transmission line (cf. column 1, lines 12-23).

Combination of said teaching with said invention is easily achieved through adding another transmission line on the opposite side of the ground plate in Steensma.

Furthermore, it would have been obvious to include further limitation (b) in view of Kuroda et al, who teach in a patent on the reduction of unwanted impedance deviations in a multi-layer wiring board, - hence closely related art, that the hole size should be selected in a range determined by an inequality satisfied for any hole size between zero and a certain maximum value, said maximum value being determined by:

$R_y \leq 25.98\ R_x^{-0.3871} - 4.370$; here R_y is the width of the ground plate divided by the signal line width and R_x is the ratio of the square of the hole size divided by ground plate width expressed in percentage; said inequality is satisfied provided for any given ground plate width and signal width the hole size is small enough, while from Figure 2 it follows that the dependence of the maximum deviation of the impedance on the open area ratio R_x defined above is characterized by a monotonically increasing function: i.e., the lower the open area ratio, the lower the (harmful) maximum deviation of the impedance can be made (cf. col. 3, l. 12-25). Although in the particular examples provided by Kuroda et al the hole size still exceeds the signal width, it would have been obvious to exploit the range as recommended by Kuroda et al in the small hole size in

view of Buuck et al, who, in a patent drawn to the setting of an impedance in a signal (transmission) line, - hence analogous art, teach that the hole size to be selected is a function of required signal band width: for wider signal bands smaller holes are required.

Motivation to adhere to the above inequality taught by Kuroda et al within the context of the invention by Steensma derives from the stated goal of tuning the impedance by Steensma (cf. col. 1, l. 24-38) while *motivation* to teach the invention by Steensma as adapted to wide band signal applications follows from the consequent increase in utility of the invention. The teaching by Kuroda et al and Buuck et al easily combines with the invention by Steensma because the selection of the size of holes presents no difficulty to those of ordinary skills.

9. ***Claim 2*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Phelan (3,771,075) (previously made of record) in view of Kuroda et al (5,479,138) and Buuck et al (5,568,107).

Phelan teaches (cf. Figure 2):

a signal line 10 (cf. column 2, lines 37-49);

a ground plate 13 (cf. column 2, lines 37-49); and

another signal line 11 (cf. column 2, lines 37-49) close to said signal line and on an opposite side of said ground plate as said signal line ;

wherein at least one through hole 14 (cf. column 2, line 49) is formed in said ground plate; and an inner wall is only directly electrically connected to said signal line by virtue of being a slot, i.e., open space (cf. column 3, lines 15-20).

Phelan does not necessarily teach the further limitation that the aperture size of said through hole to be smaller than a width of said signal line.

However, it would have been obvious to include said further limitation in view of Kuroda et al, who teach in a patent on the reduction of unwanted impedance deviations in a multi-layer wiring board, - hence closely related art, that the hole size should be selected in a range determined by an inequality satisfied for any hole size between zero and a certain maximum value, said maximum value being determined by:

$R_y \leq 25.98\ R_x^{-0.3871} - 4.370$; here R_y is the width of the ground plate divided by the signal line width and R_x is the ratio of the square of the hole size divided by ground plate width expressed in percentage; said inequality is satisfied provided for any given ground plate width and signal width the hole size is small enough, while from Figure 2 it follows that the dependence of the maximum deviation of the impedance on the open area ratio R_x defined above is characterized by a monotonically increasing function: i.e., the lower the open area ratio, the lower the (harmful) maximum deviation of the impedance can be made (cf. col. 3, l. 12-25). Although in the particular examples provided by Kuroda et al the hole size still exceeds the signal width, it would have been obvious to exploit the range as recommended by Kuroda et al in the small hole size in view of Buuck et al, who, in a patent drawn to the setting of an impedance in a signal (transmission) line, - hence analogous art, teach that the hole size to be selected is a function of required signal band width: for wider signal bands smaller holes are required.

Motivation to adhere to the above inequality taught by Kuroda et al within the context of the invention by Phelan derives from the stated undesirability of impedance

mismatch in Phelan (cf. col. 3, l. 50-60) while *motivation* to teach the invention by Phelan as adapted to wide band signal applications follows from the consequent increase in utility of the invention. Over a wide range the selection of hole size does not present any difficulty at all for those of ordinary skills in the art; therefore, the teachings by Kuroda et al and Buuck et al may be easily *combined* with the invention by Phelan.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
July 9, 2004

Johannes Mondt
Patent Examiner, Art Unit 2826